IN THE CLAIMS

Please amend claims 1 and 20, as set forth below.

Please cancel claims 6-7 and 24-25, as set forth below.

The text of all pending claims, along with their current status, is set forth below:

1. (Currently Amended) A plurality of generally elliptical capacitive memory elements, each capacitive memory element having a first electrode with an interior portion forming a pair of concentric sidewalls extending perpendicularly from a substrate, the plurality of capacitive memory elements disposed on the ~~a~~ substrate so that an axis that runs longitudinally through one of the plurality of capacitive memory elements is not generally parallel with an edge of the substrate.

2. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein the axis is not generally perpendicular with an orthogonal edge of the substrate.

3. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein the substrate comprises a processor.

4. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein the substrate comprises a memory device.

5. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein the substrate comprises an integrated circuit device.

6-7. (Canceled)

8. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein each of the plurality of capacitive memory elements is slanted with respect to the edge of the substrate.

9-19. (Withdrawn)

20. (Currently Amended) An integrated circuit device, comprising:

a substrate;

a memory array that includes a plurality of memory cells disposed on the substrate, the memory array comprising a plurality of capacitive memory elements, each of the capacitive memory elements being associated with one of the plurality of memory cells, each capacitive memory element having a first electrode with an interior portion forming a pair of concentric sidewalls extending perpendicularly from the substrate, the plurality of capacitive memory elements being disposed on the substrate so that an axis that runs longitudinally through one of the plurality of capacitive memory elements is not generally parallel with an edge of the substrate.

21. (Original) The integrated circuit device set forth in claim 20 wherein the axis is not generally perpendicular with an orthogonal edge of the substrate.

22. (Original) The integrated circuit device set forth in claim 20 wherein the substrate comprises a processor.

23. (Original) The integrated circuit device set forth in claim 20 wherein the substrate comprises a memory device.

24-25. (Canceled)

26. (Original) The integrated circuit device set forth in claim 20 wherein each of the plurality of capacitive memory elements is slanted with respect to the edge of the substrate.

27-36. (Withdrawn)

37-57. (Canceled)

58. (Withdrawn)

59. (Withdrawn)